CURTISS-WRIGHT

Defense Solutions Division

Ensuring Product Integrity with Truly Open Solutions

Steve Edwards and Ivan Straznicky

FABRIC40™

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Ensuring Product Integrity with Truly Open Solutions

- Steve Edwards will discuss:
  - The challenges and solutions for ensuring product integrity for 10 Gbaud backplanes and beyond
  - The problem of processor “throttling”, which can detrimentally affect determinism in control systems.
- Ivan Straznicky will discuss:
  - Advanced cooling techniques to mitigate throttling that adhere to and extend VITA standards (vs. proprietary approaches) while also supporting RAND licensing models.

Ensuring product integrity for 10 Gbaud and beyond

Steve Edwards, Technical Fellow, Dir. Product Management – ISR Solutions

Ensuring product integrity for 10 Gbaud backplanes and beyond

VITA
Open Standards, Open Markets

MULTIBUS

VME64

VPX

FABRIC40™

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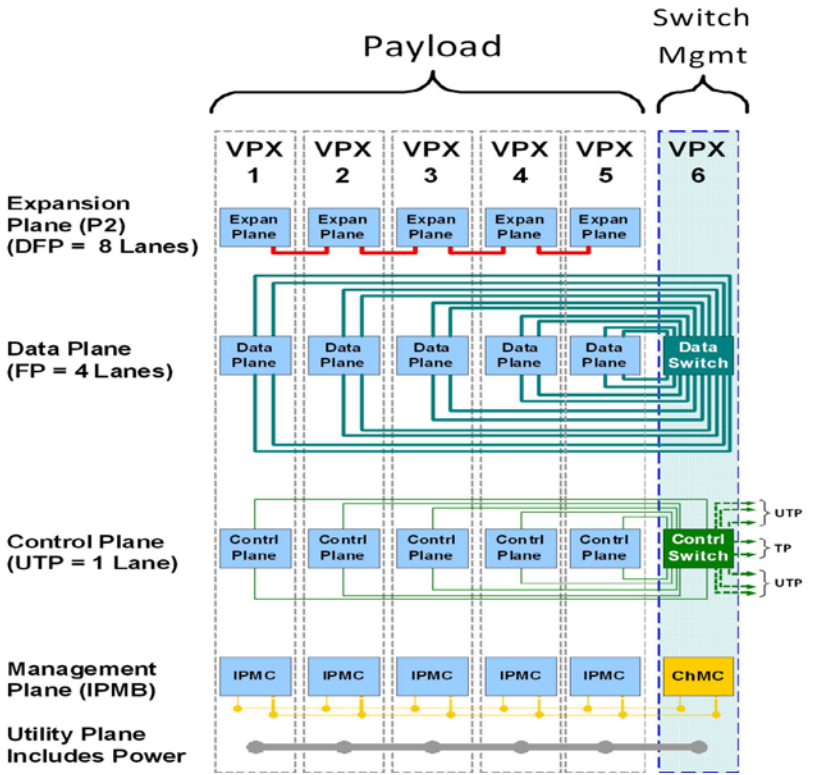
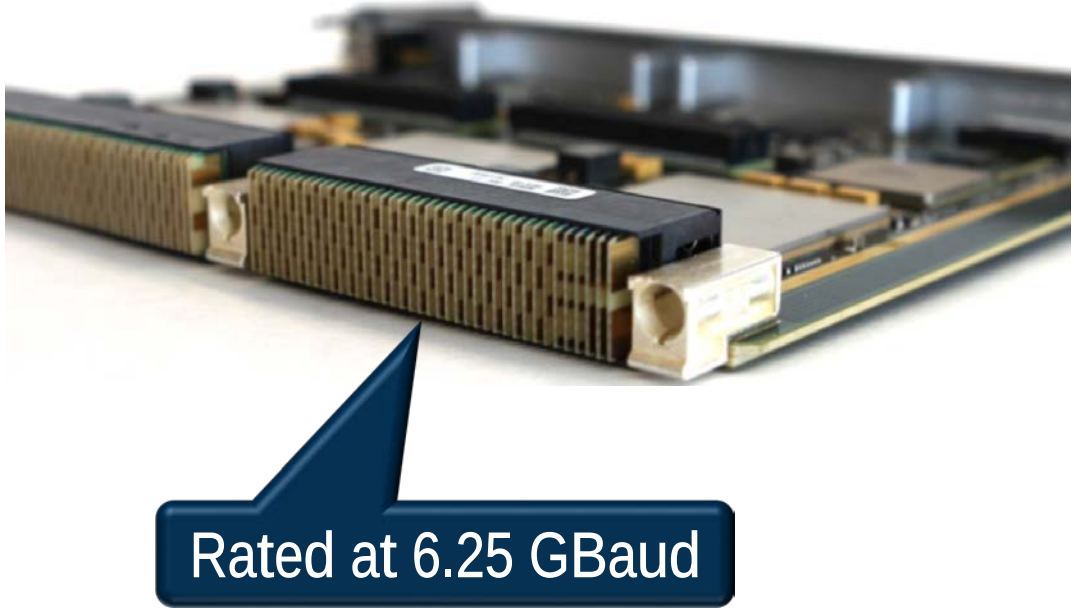
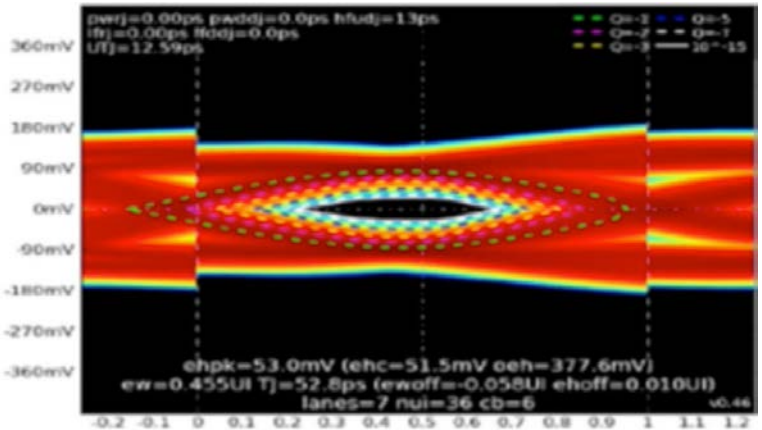
Ensuring product integrity for 10 Gbaud backplanes and beyond



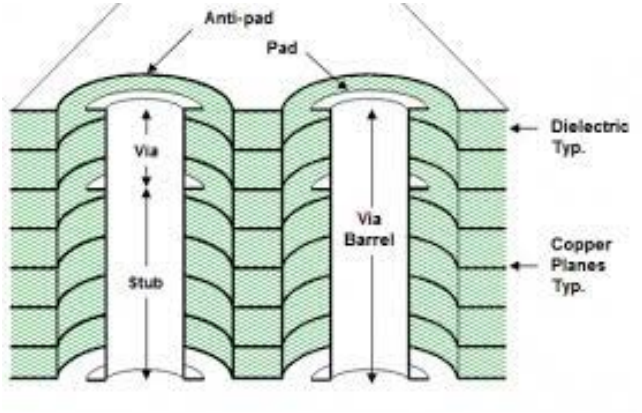


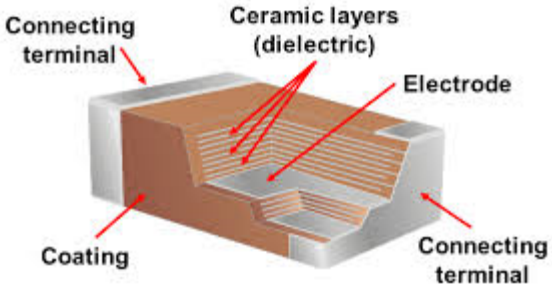
10.3 Gbaud 6-slot Central Switch Backplane

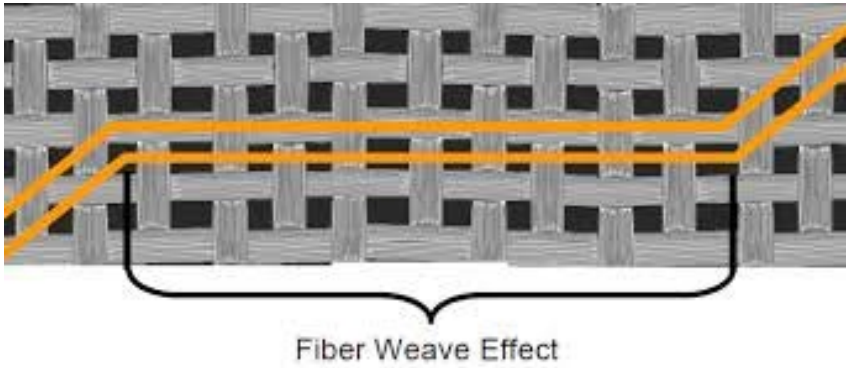
Ensuring product integrity for 10 Gbaud backplanes and beyond



Almost closed eye @ 10.3Gbaud

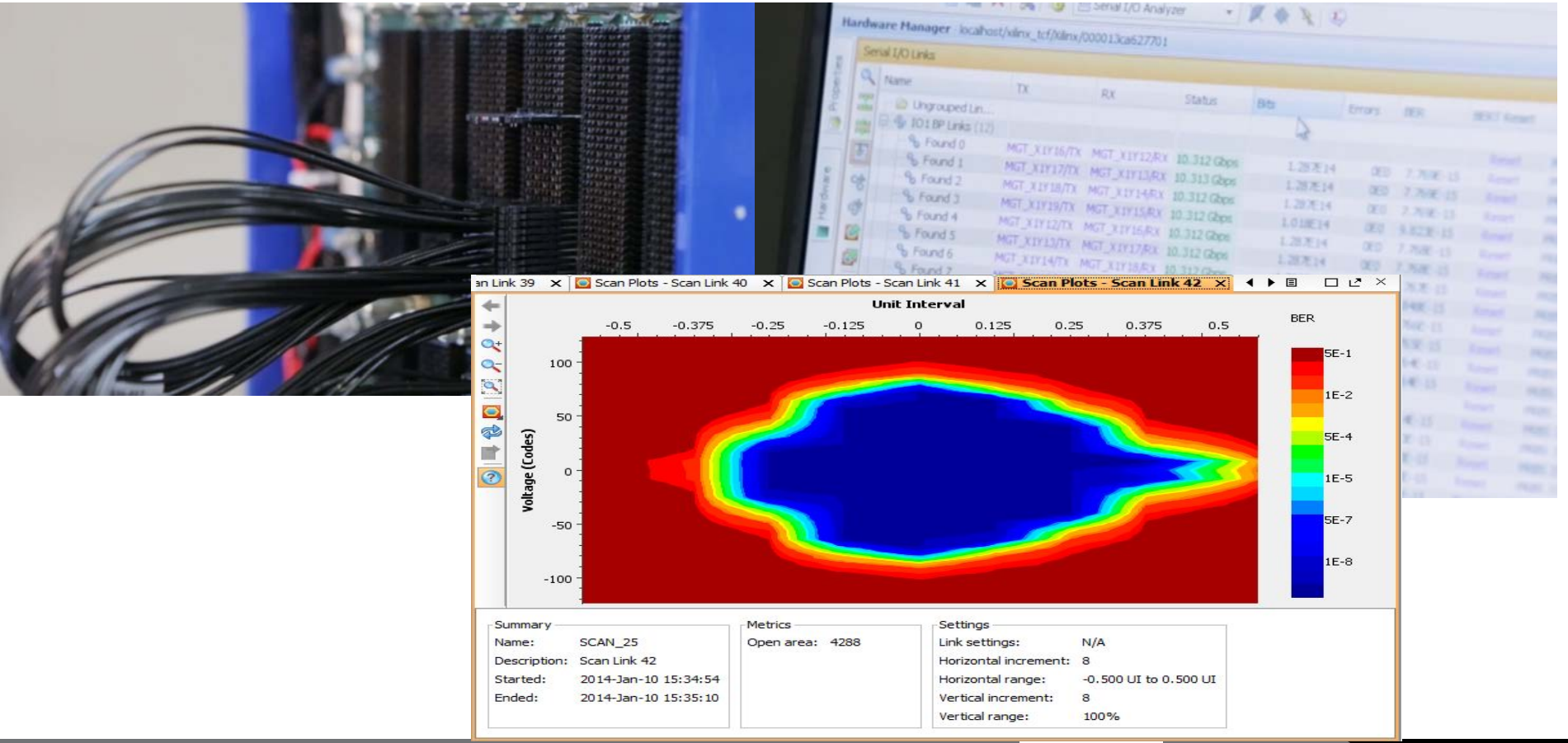






Fiber Weave Effect

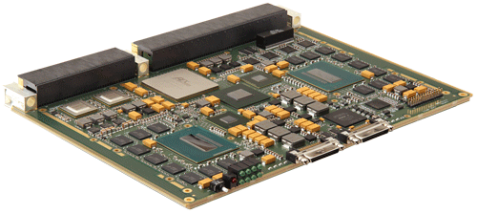
Ensuring product integrity for 10 Gbaud backplanes and beyond



Ensuring product integrity for 10 Gbaud backplanes and beyond

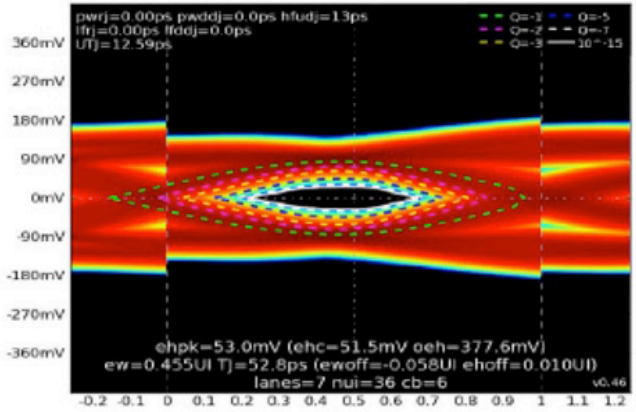
Profile name	Data Plane 4 FP				Expansion Plane	Control Plane 2 UTPs		Control Plane 2 TPs	
	DP01	DP02	DP03	DP04		CPutp01	CPutp02	CPtp01	CPtp02
MOD6-PAY-4F1Q2U2T-12.2.1-1	SRIO 1.3 at 3.125 Gbaud				PCIe Gen 1	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-2	SRIO 1.3 at 3.125 Gbaud				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-3	PCIe Gen 1				PCIe Gen 1	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-4	PCIe Gen 2				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-5	10GBASE-BX4				PCIe Gen 1	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-6	10GBASE-BX4				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-7	10GBASE-KX4				PCIe Gen 1	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-8	10GBASE-KX4				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-9	SRIO 2.0 at 5.0 Gbaud				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-10	SRIO 2.0 at 6.25 Gbaud				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-11	SRIO 2.1 at 5.0 Gbaud				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-12	SRIO 2.1 at 6.25 Gbaud				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-13	InfiniBand DDR				PCIe Gen 3	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-14	40GBase-KR4				PCIe Gen 2	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-15	40GBase-KR4				PCIe Gen 3	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-16	InfiniBand QDR				PCIe Gen 3	1000BASE-BX		1000Base-T	
MOD6-PAY-4F1Q2U2T-12.2.1-17	InfiniBand FDR				PCIe Gen 3	1000BASE-BX		1000Base-T	

Proposed Gen 3 Data Rates

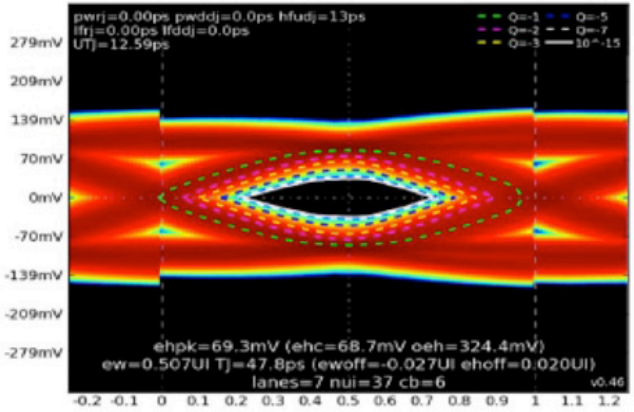


Ensuring product integrity for 10 Gbaud backplanes and beyond

Industry Design Rules
provide insufficient margin



Curtiss-Wright Design Rules
provide superior margin



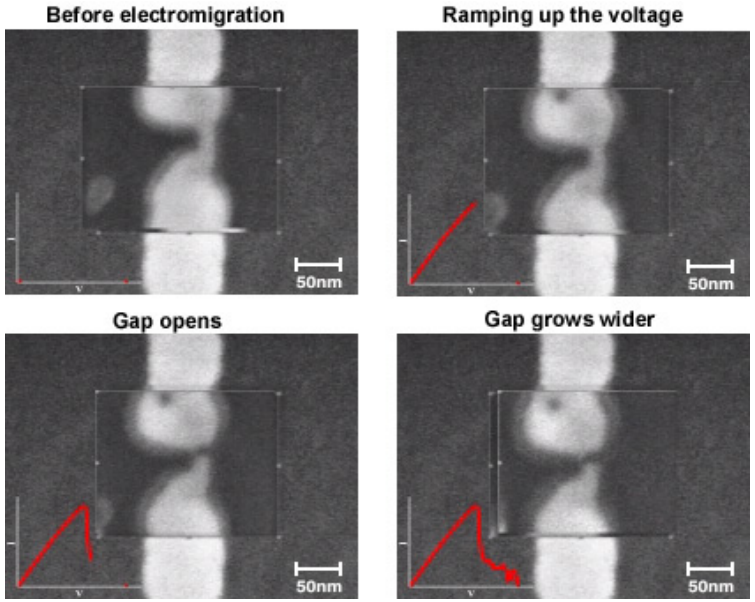
Advanced cooling techniques for High-Speed Systems

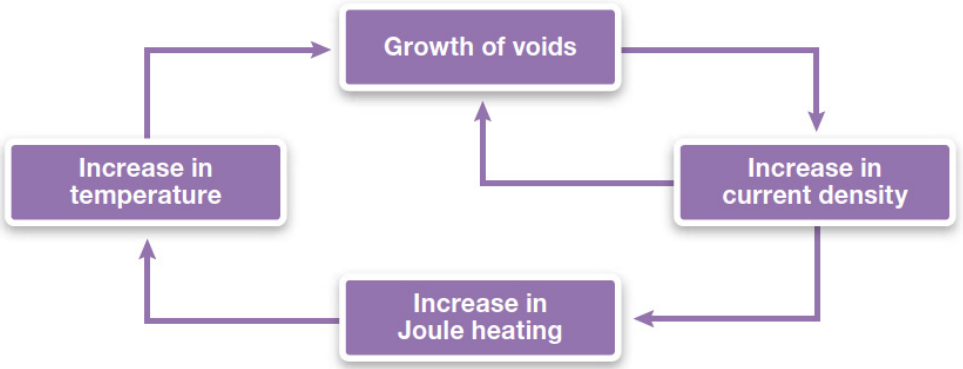
Ivan Straznicky, Technical Fellow, Curtiss-Wright Defense Solutions

HPC/HPEC


CURTISS WRIGHT
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PLATFORM CONTROL
PMBus
SYS RESET
ESD
DC ENABLE/ INHIBIT

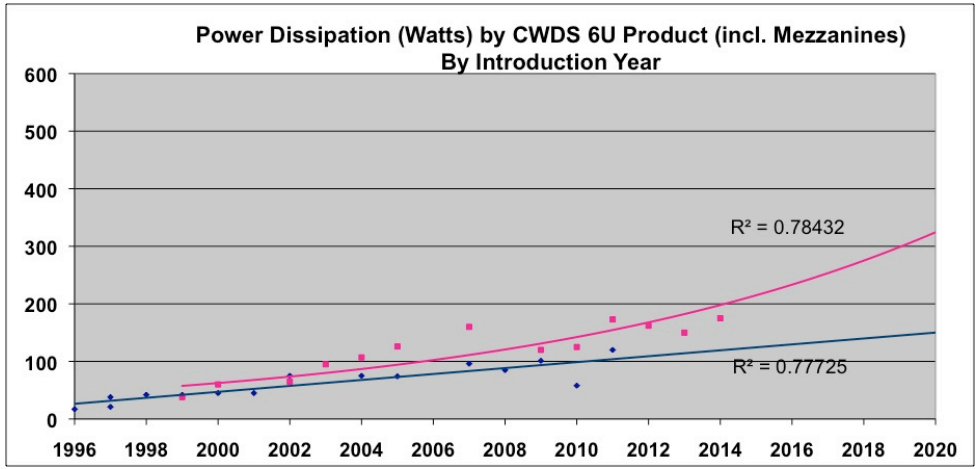
Electromigration





Thermal Management Overview

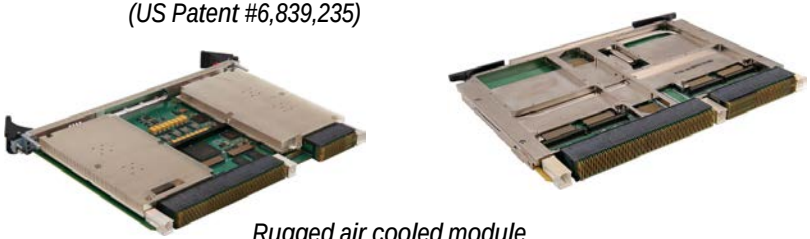
- Open standards based modules & chassis with innovative cooling



Liquid flow through module (US Patent #7,515,418)

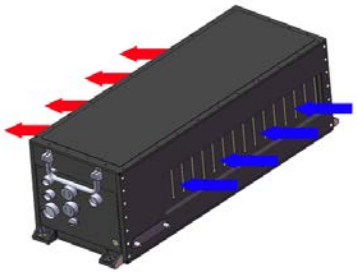
Air flow through module

Rugged conduction module with embedded heat pipes (US Patent #6,839,235)



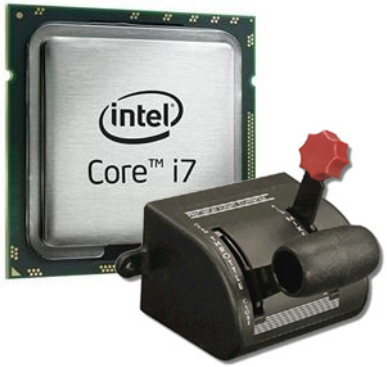
Rugged air cooled module

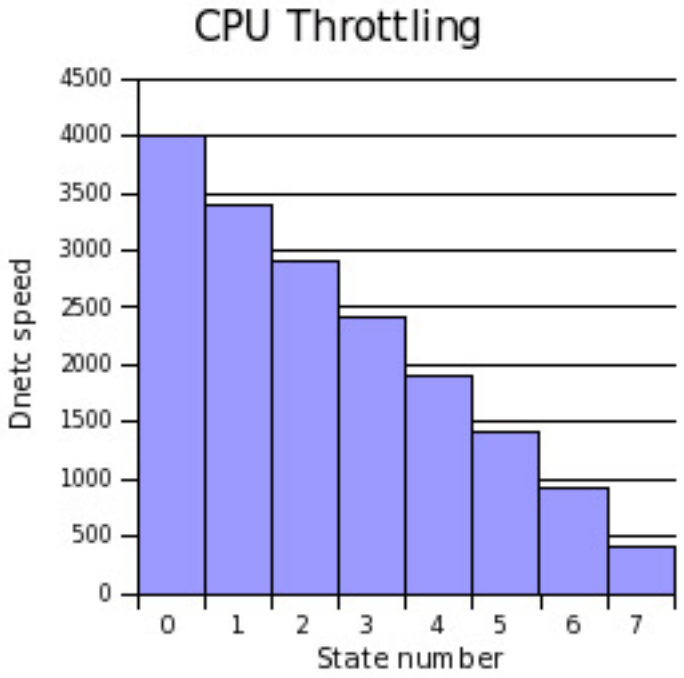
Liquid cooled sidewall chassis (>100W/slot) – Patent pending



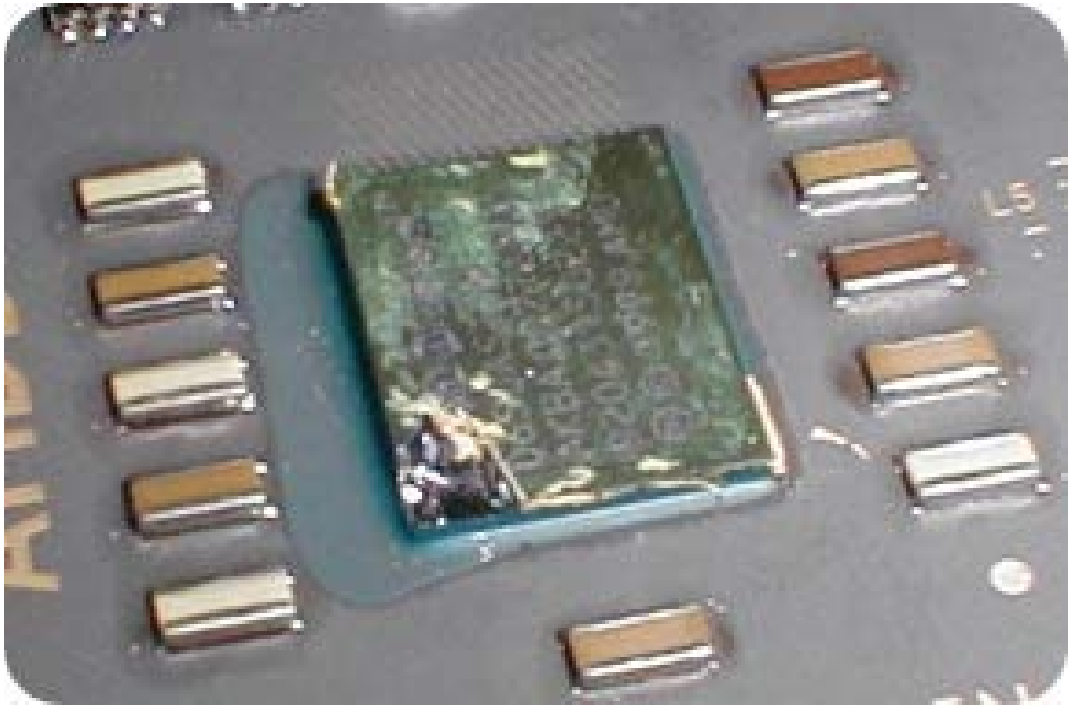
Air flow through chassis

CPU Throttling

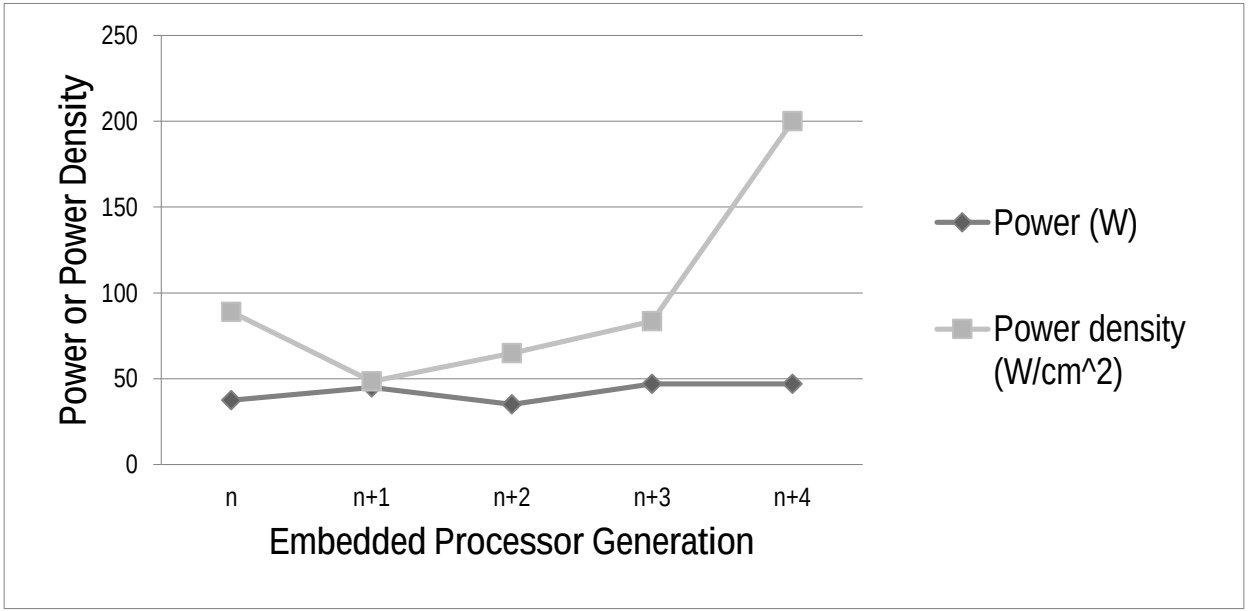




Thermal Runaway



Processor Power / Power Density



Air vs. Liquid

High Power Conduction (up to 470W)

The End

Q&A

www.cwcdefense.com